



FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-060 APPLICANT(S): Lochtefeld <i>et al.</i> SERIAL NO.: 10/691,007 FILING DATE: October 22, 2003 GROUP: 2812
--	---

U.S. PATENT DOCUMENTS

EXAM. INIT.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
26	A1	5,227,664	07/13/1993	Ueno		
	A2	6,268,253 B1	07/31/2001	Yu		
	A3	6,383,879 B1	05/07/2002	Kizilyalli <i>et al.</i>		
	A4	6,429,061 B1	08/06/2002	Rim		
26	A5	2002/0076886 A1	060/20/2002	Rotondaro <i>et al.</i>		

FOREIGN PATENT DOCUMENTS

EXAM. INIT.	DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
26	B1	0 784 339 A2	07/16/1997	EP			No	Yes
26	B2	01/93338 A1	12/06/2001	WO			No	Yes

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
26	C1	Imai <i>et al.</i> (May, 2002) "A 100 nm Node CMOS Technology for System-on-a-Chip Applications", <u>IEICE Trans. Electron.</u> , Vol. E85-C, No. 5, pp. 1057-1063.
	C2	Park <i>et al.</i> (2002) "Gate Postdoping to Decouple Implant/Anneal for Gate, Source/Drain, and Extension: Maximizing Polysilicon Gate Activation for 0.1 μ m CMOS Technologies", <u>2002 Symposium on VLSI Technology Digest of Technical Papers</u> , pp. 134-135.
	C3	Reinking <i>et al.</i> (March, 1999) "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates", <u>Electronics Letters</u> , Vol. 35, No. 6, pp. 503-504.
	C4	Rim <i>et al.</i> (2002) "Characteristics and Device design of Sub-100 nm Strained SI N-and PMOSFETs", <u>2002 Symposium on VLSI Technology Digest of Technical Papers</u> , pp. 98-99.
26	C5	Su <i>et al.</i> (2000) "Strained Si _{1-x} Ge _x graded channel PMOSFET grown by UHVCVD", <u>Thin Solid Films</u> , Elsevier Science, Vol. 369, No. 1-2, pp. 371-374.

EXAMINER <i>K. P. ...</i>	DATE CONSIDERED <i>3/16/05</i>

FORM PTO - 1449				ATTORNEY DOCKET NO.: ASC-060					
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT				APPLICANT(S): Lochtefeld <i>et al.</i>					
				SERIAL NO.: 10/691,007					
				FILING DATE: October 22, 2003					
				GROUP: 2812					
U.S. PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE		
FOREIGN PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
27	C6	Takagi <i>et al.</i> (August, 2001) "Strained-Si-on-Insulator (Strained-SOI) MOSFETs-Concept, Structures and Device Characteristics", IEICE Trans. Electron., Vol. E84-C, No. 8, pp. 1043-1050.							
	C7	Wyon (2002) "Future technology for advanced MOS devices", <u>Nuclear Instruments & Methods in Physics Research, Section - B: Beam Interactions With Materials and Atoms</u> , North-Holland Publishing Company, Amsterdam, NL, Vol. 186, No. 1-4, pp. 380-391.							
	C8	Xiang <i>et al.</i> (2000) "Very High Performance 40nm CMOS with Ultra-thin Nitride/Oxynitride Stack Gate Dielectric and Pre-doped Dual Poly-Si Gate Electrodes", <u>International Electron Devices Meeting 2000 IEDM Technical Digest</u> , pp. 860-862.							
4	C9	International Search Report for PCT/US03/33561, dated 3/24/2004							
EXAMINER K.P. CARP					DATE CONSIDERED 3/16/05				

3048595